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EXAMINER

FINDLEY, CHRISTOPHER G

ART UNIT

PAPER NUMBER

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/799,032	<b>Applicant(s)</b> HATTI ET AL.	
	<b>Examiner</b> CHRISTOPHER FINDLEY	<b>Art Unit</b> 2482	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2,5,6 and 8-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,6 and 8-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)         | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed 8/09/2010 have been fully considered but they are not persuasive.
2. Re claim 1, the Applicant contends that where the "a data word packing a first pixel, followed immediately by a second pixel, followed immediately by a third pixel, followed immediately by a fourth pixel", the first and second pixels are not swapped with each other, and the third and fourth pixels are not swapped with each other in the prior art cited. However, the Examiner respectfully disagrees. Baden discloses that servicing a frame buffer read operation involves using the pixel depth 511 to decide how to swap the pixels shown in block 521 to arrive at the corresponding pixels depicted in block 519 (Baden: Fig. 5 and column 15, lines 42-45), wherein the read operation is a reverse adaptation of the write operation (Baden: column 15, lines 39-42).
3. Re claim 9, the Applicant contends that the prior art cited fails to teach or suggest "providing the portion of the picture with the particular pixel order and providing the portion of the picture with the predetermined pixel order". However, the Examiner respectfully disagrees. Baden discloses that the data is provided to the system data bus conditionally according to desired mode (Baden: column 15, lines 51-55).
4. Re claim 5, the Applicant contends that the prior art cited fails to teach or suggest "a decompression engine for decompressing compressed video data and writing decompressed video data to a frame buffer with a byte order, said decompressed video data comprising a picture". The Examiner concedes that the prior art previously cited fails to disclose this limitation. However, the Examiner notes that this language is newly added to the claim and has been addressed below by the additional citation of Ho et al. (US 5428741 A).

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2482

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**6. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Baden et al. (US 5640545 A).**

Re **claim 1**, Baden discloses a method for displaying pictures, said method comprising: fetching a portion of a picture being stored in a frame buffer, the portion of the picture stored with a byte order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); converting the byte order of the portion of the picture to a predetermined byte order, the byte order being different from the predetermined byte order (Baden: Fig. 6, multiplexer 649; column 15, lines 51-55, the processor determines the byte order of the system data bus; column 16, lines 35-43, multiplexer 649 performs end-to-end byte swapping according to the mode of the input byte order in relation to the processor byte order); and storing the portion of the picture in another buffer with the predetermined byte order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); providing an indicator indicating whether the byte order is different or opposite from the predetermined order that the portion of the picture is converted (Baden: column 16, lines 50-53, the controller generates a little-endian or big-endian control signal, acting as a state machine, wherein the control signal is generated based on information about the processor mode, thus indicating whether a conversion is necessary); from a data word packing a first pixel, followed immediately by a second pixel, followed immediately by a third pixel, followed immediately by a fourth pixel: swapping a first pixel from the portion of the picture and a second pixel from the portion of the picture with each other if the indicator indicates that the byte order is different or opposite from the predetermined order (Baden: Fig. 5 and column 15, lines 42-45, servicing a frame buffer read operation involves using the pixel depth 511 to decide how to swap the pixels shown in block 521 to arrive at the corresponding pixels depicted in block 519; column 15, lines 39-42, wherein the read operation is a reverse adaptation of the write operation); and swapping a third pixel from the portion of the picture and a fourth pixel with each other from the portion of the picture if the indicator indicates that the byte order is different or opposite from the predetermined order (Baden: Fig. 5 and column 15, lines 42-45, servicing a frame buffer read operation

Art Unit: 2482

involves using the pixel depth 511 to decide how to swap the pixels shown in block 521 to arrive at the corresponding pixels depicted in block 519; column 15, lines 39-42, wherein the read operation is a reverse adaptation of the write operation).

Re **claim 2**, Baden discloses that the predetermined order is selected from a group consisting of big endian byte order and little endian byte order (Baden: column 15, lines 51-55, the processor determines big-endian (BE) or little-endian (LE) mode).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claims 9-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A).**

Re **claim 9**, Baden discloses a method for displaying pictures, said method comprising: fetching a portion of a picture stored in a frame buffer, the portion of the picture being stored with a pixel order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data; Figs. 2A-2B, bytes correspond to color pixels); converting the pixel order of the portion of the picture to a predetermined pixel order (Baden: Fig. 6, multiplexer 649; column 15, lines 51-55, the processor determines the byte order of the system data bus; column 16, lines 35-43, multiplexer 649 performs end-to-end byte swapping according to the mode of the input byte order in relation to the processor byte order); and storing the portion of the picture in another buffer with the predetermined pixel order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data; Figs. 2A-2B, bytes correspond to color pixels); and providing the portion of the picture with the particular pixel order and providing the portion of the picture with the predetermined pixel order (Baden: column 15, lines 51-55, data is provided to the system data bus conditionally according to desired mode).

Art Unit: 2482

While Baden does not explicitly disclose that memory subsystem 309 stores a picture, Baden does disclose that a system bus in conventional computer graphics systems in the same field of endeavor as the prior art conveys both address and pixel data information (Baden: column 1, lines 21-23). Memory subsystem 309 and processor 307 are the only components explicitly shown as being connected along system data bus 305 of Fig. 3 in Baden. Since the input to the bridge/graphics controller 311 is coupled to the system data bus 305, as noted by the Applicant, one of ordinary skill in the art at the time of the invention would have found it obvious that picture data is stored in the memory subsystem 309 because a processor by itself does not store data, and therefore, in view of the disclosed figures of Baden, the memory subsystem 309 must store the data by default.

Re **claim 10**, Baden discloses receiving an indicator indicating the pixel order (Baden: Fig. 7A, mode selection line 655); and selecting one of the portion of the picture with the particular pixel order and the portion of the picture with the predetermined order based on the indicator indicating the pixel order (Baden: column 15, lines 51-55, data is provided to the system data bus conditionally according to desired mode).

**Claim 11** recites the corresponding system for implementing the method of claim 9, and, therefore, has been analyzed and rejected with respect to claim 9 above.

**9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A) in view of Ho et al. (US 5428741 A).**

Re **claim 5**, Baden discloses a system for displaying pictures, said system comprising: a first circuit for fetching a portion of a picture stored in the frame buffer with the byte order (Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); a second circuit for converting the byte order of the portion of the picture to a predetermined byte order, the byte order being different from the predetermined byte order (Baden: Fig. 6, multiplexer 649; column 15, lines 51-55, the processor determines the byte order of the system data bus; column 16, lines 35-43, multiplexer 649 performs end-to-end byte swapping according to the mode of the input byte order in relation to the processor byte order); and a buffer for storing the portion of the picture with the predetermined byte order

Art Unit: 2482

(Baden: Fig. 6, flip flops 623 and 625; column 15, line 64, through column 16, line 4, flip flops buffer data); and a state machine for providing an indicator indicating whether the byte order is different or opposite from the predetermined order that the portion of the picture is converted to the second circuit (Baden: column 16, lines 50-53, the controller generates a little-endian or big-endian control signal, acting as a state machine, wherein the control signal is generated based on information about the processor mode, thus indicating whether a conversion is necessary).

Baden does not explicitly disclose a decompression engine for decompressing compressed video data and writing decompressed video data to a frame buffer with a byte order, said decompressed video data comprising a picture. However, Ho discloses a high-speed image preprocessing system including a multi-purpose buffer for storing digital image data, wherein the image preprocessing system may perform byte swapping and data decompression (Ho: column 2, lines 47-49). Since both Baden and Ho relate to image processing including byte swapping, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the decompression capabilities of Ho with the system of Baden in order to optimize processor workload by providing a system that can both perform decompression as well as offload operations to external devices which may utilize different byte orders.

**Claim 6** has been analyzed and rejected with respect to claim 2 above.

**10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A) in view of Wyland (US 6836869 B1).**

Re **claim 12**, Baden discloses a majority of the features of claim 11 as discussed above, including performing an end-to-end byte swapping operation, but Baden does not specifically disclose a demultiplexer for separating a plurality of pixels from the portion of the picture; a plurality of multiplexers for combining the separated plurality of pixels in a corresponding plurality of pixel orders; and another multiplexer for selecting an output from one of the plurality of multiplexers, based on an indicator indicating the pixel order provided by the state machine. However, Wyland discloses a byte swapping unit, wherein a 32-bit input stream is demultiplexed into four 8-bit bytes, and the bytes are fed into four 2-input multiplexers, so that the bytes may be swapped in an end-to-end manner based on a

Art Unit: 2482

byte\_endian\_type control signal, whereby the output of the multiplexers are then recombined into a 32-bit stream (Wyland: Fig. 5A). Since both Baden and Wyland relate to performing byte swapping, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the multiplexer configuration of Wyland with the bridge/graphics controller of Baden in order to provide a system which is capable of operating in both an encoding/decoding mode and error correction mode while utilizing a single circuit configuration (Wyland: column 2, lines 14-17). The combined system of Baden and Wyland has all of the features of claim 12.

**11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baden et al. (US 5640545 A) in view of Ho et al. (US 5428741 A) in view of Wyland (US 6836869 B1).**

Re **claim 8**, Baden discloses a majority of the features of claim 8 as discussed above, including performing an end-to-end byte swapping operation, but Baden does not specifically disclose a first multiplexer for selecting one of a first pixel of the portion of the picture and a second pixel of the portion of the picture; a second multiplexer for selecting another of the first pixel of the portion of the picture and a second pixel of the portion of the picture, from the first multiplexer; a third multiplexer for selecting one of a third pixel of the portion of the picture and a fourth pixel of the portion of the picture; a fourth multiplexer for selecting another of the third pixel of the portion of the picture and the fourth pixel of the portion of the picture, from the third multiplexer; a fifth multiplexer for multiplexing outputs from the first multiplexer, the second multiplexer, the third multiplexer, and fourth multiplexer; and the selections of the first multiplexer, the second multiplexer, the third multiplexer, and the fourth multiplexer being controlled by the indicator provided by the state machine. However, Wyland discloses a byte swapping unit, wherein a 32-bit input stream is demultiplexed into four 8-bit bytes, and the bytes are fed into four 2-input multiplexers, so that the bytes may be swapped in an end-to-end manner based on a byte\_endian\_type control signal, whereby the output of the multiplexers are then recombined into a 32-bit stream (Wyland: Fig. 5A). Since both Baden and Wyland relate to performing byte swapping, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the multiplexer configuration of Wyland with the bridge/graphics controller of Baden in order to provide a system which is capable of operating in both an



Art Unit: 2482

encoding/decoding mode and error correction mode while utilizing a single circuit configuration (Wyland: column 2, lines 14-17). The combined system of Baden and Wyland has all of the features of claim 8.

### ***Conclusion***

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### ***Contact***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER FINDLEY whose telephone number is (571)270-1199. The examiner can normally be reached on Monday-Friday (8:30 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2482

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/  
Supervisory Patent Examiner, Art Unit 2482

/Christopher Findley/